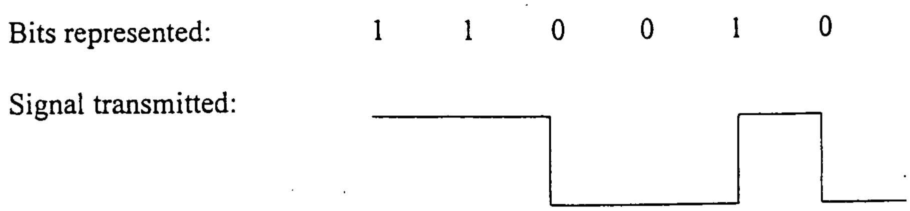

Fig. 1a

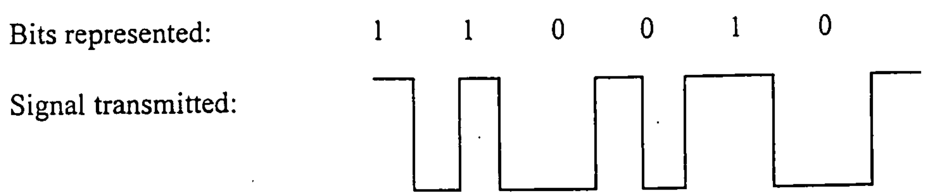

Fig. 1b

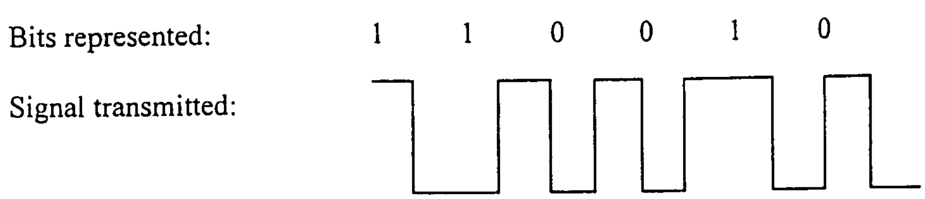

Fig. 1c

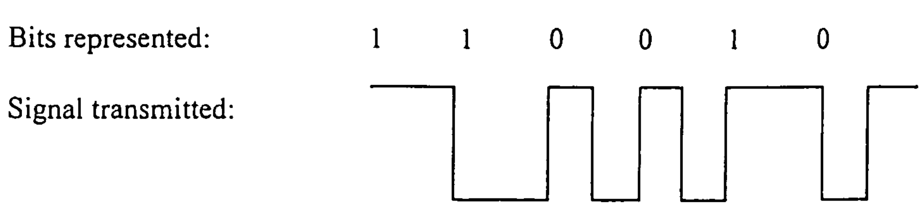

Fig. 2

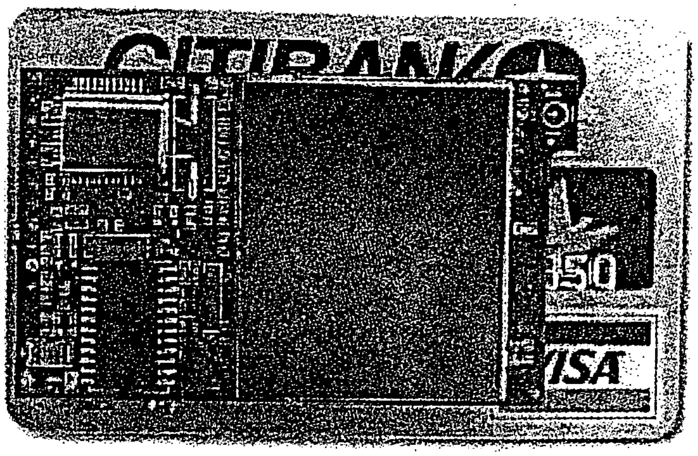

Fig. 3

J1 PIN DESCRIPTIONS

J1-1	CTS	Clear to send flow control (output)
J1-2	INT1	Interrupt line to radio processor (input, not currently implemented)
J1-3	TX	Asynchronous data output (data going from radio to user)
J1-4	RX	Asynchronous data input (data going from user to radio)
J1-5	RTS	Ready to send flow control (input, not currently implemented)
J1-6	*RESET	Reset line to radio processor (assert low to reset radio processor)
J1-7	MOSI	SPI data in (input, not currently implemented)
J1-8	MISO	SPI data out (output, not currently implemented)
J1-9	SCK	SPI data clock (input/output, not currently implemented)
J1-10	Power	+5 volts DC. (55mA in RX mode, 200mA in TX mode)
J1-11	Ground	

J2 PIN DESCRIPTIONS

J2-1	Ground
J2-2	Ground
J2-3	Ground
J2-4	Ground

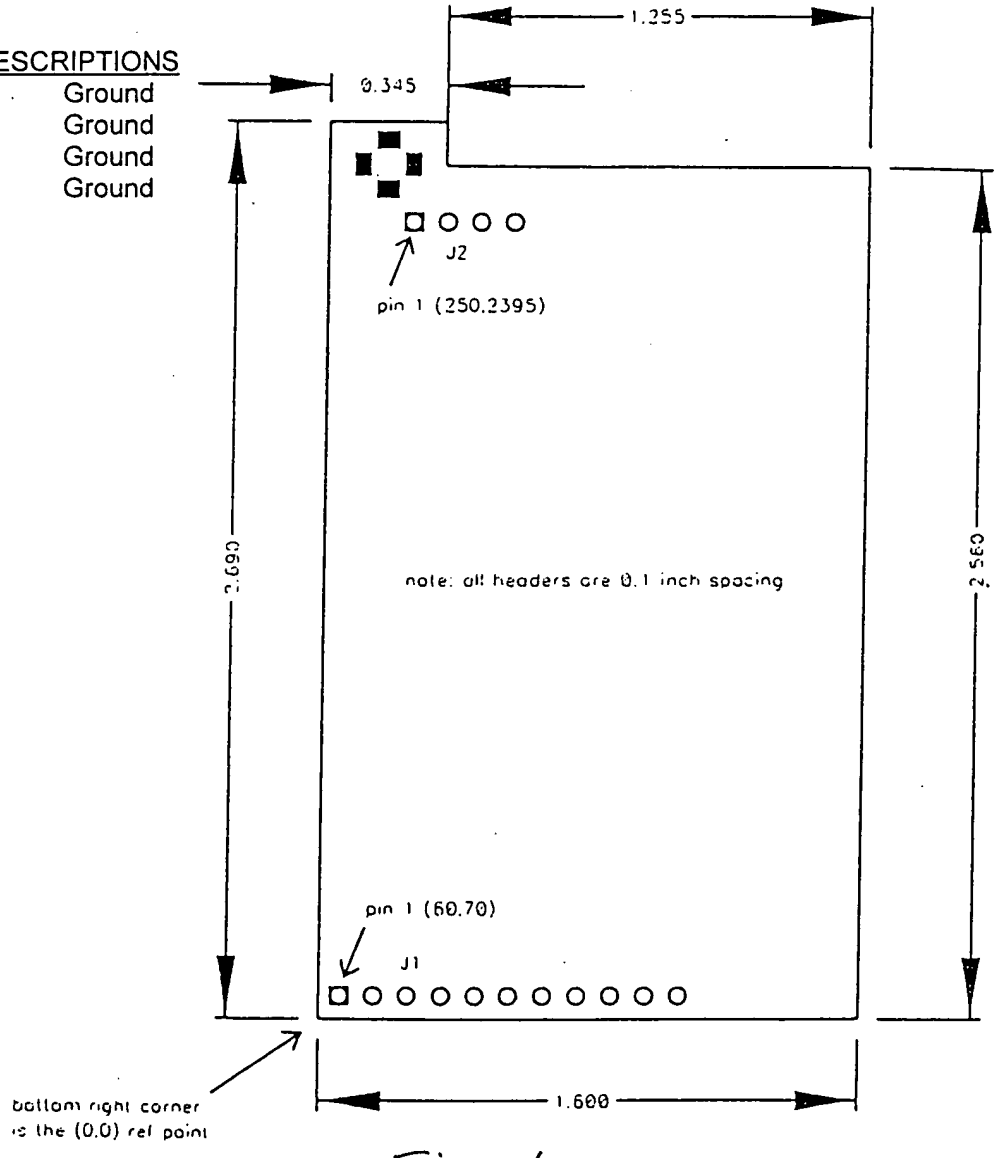

Fig. 4a

Pin	Signal	Type	Description
1	CTS	Output	Clear to send Flow control
2	PwrDn	Input	Power Down
3	RX	Output	Receive Data
4	TX	Input	Transmit Data
5	NC	-	Reserved
6	*Reset	Input	Reset radio (assert low to reset)
7-9	NC	-	Reserved
10	Vcc	Input	5 VDC, +/-0.3V
11	Gnd	-	Signal and chassis ground

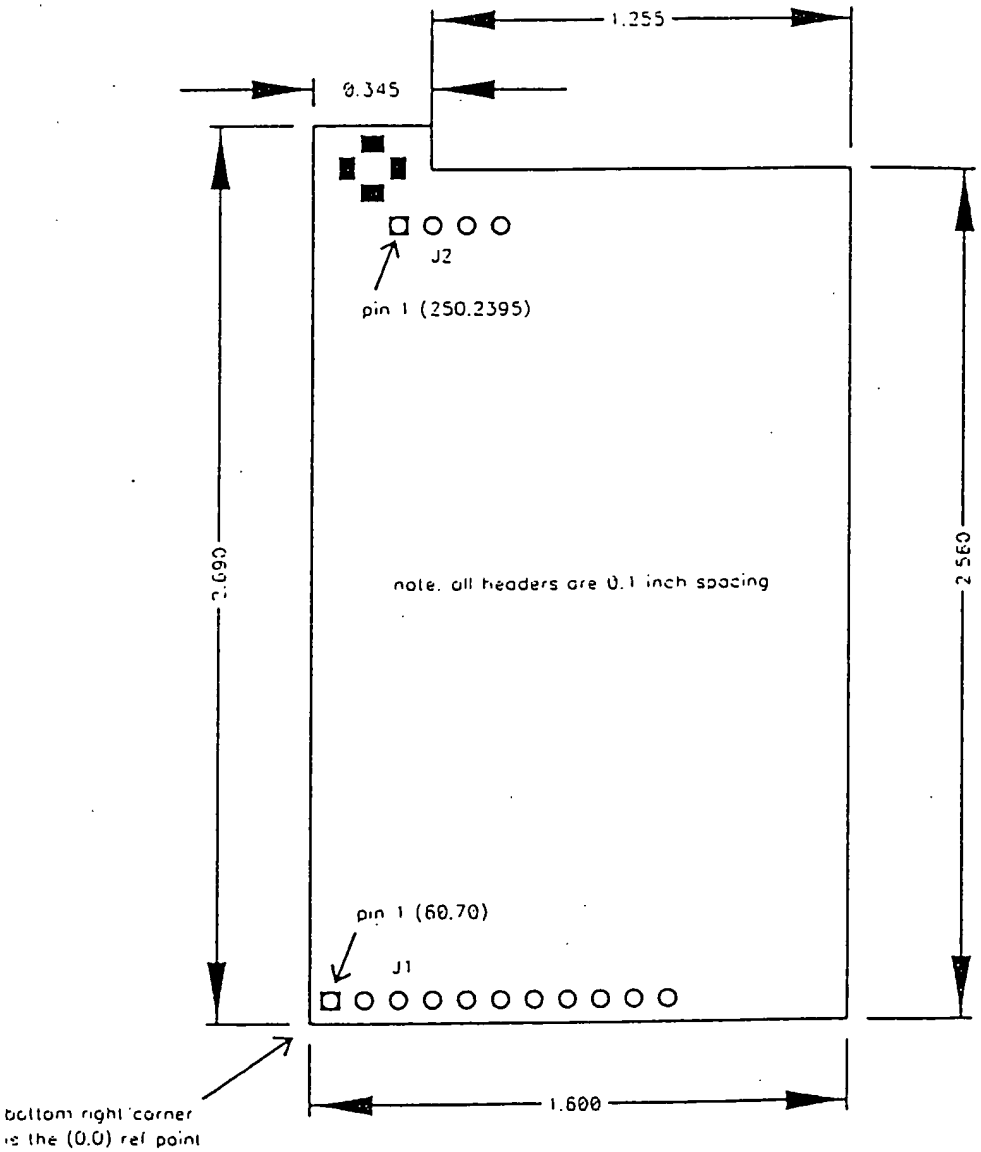

Fig. 46

Pin	Signal	Type	Description
1	CTS	Output	Clear to send flow control
2	NC		Reserved
3	RX	Output	Received Data
4	TX	Input	Data to transmit
5	NC		Reserved
6	*RESET	Input	Reset (assert low to reset radio)
7	NC		Reserved
8	NC		Reserved
9	NC		Reserved
10	VCC	Input	+5 VDC +/-0.3V (200mA)
11	GND		Signal and chassis ground

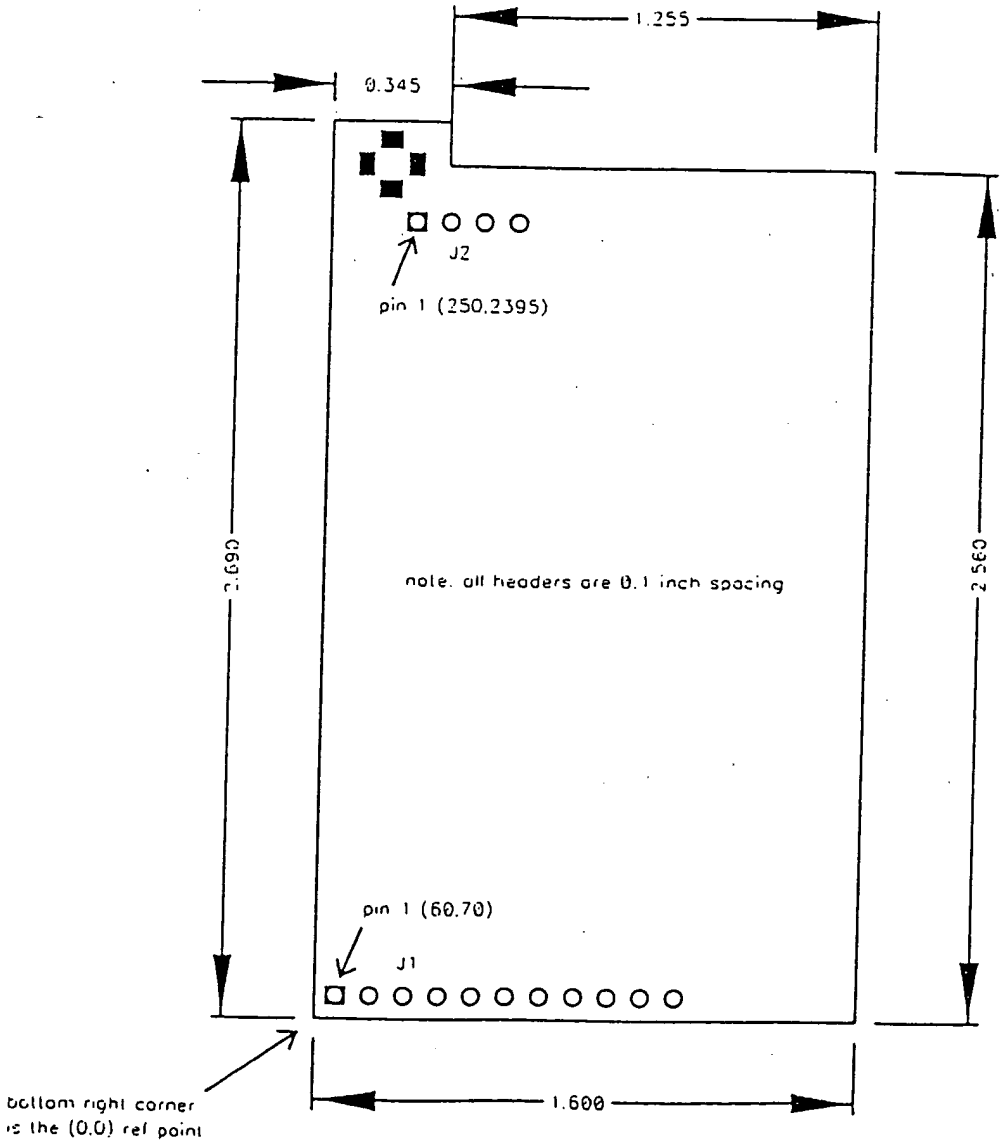

Fig. 4c

Fig. 5a

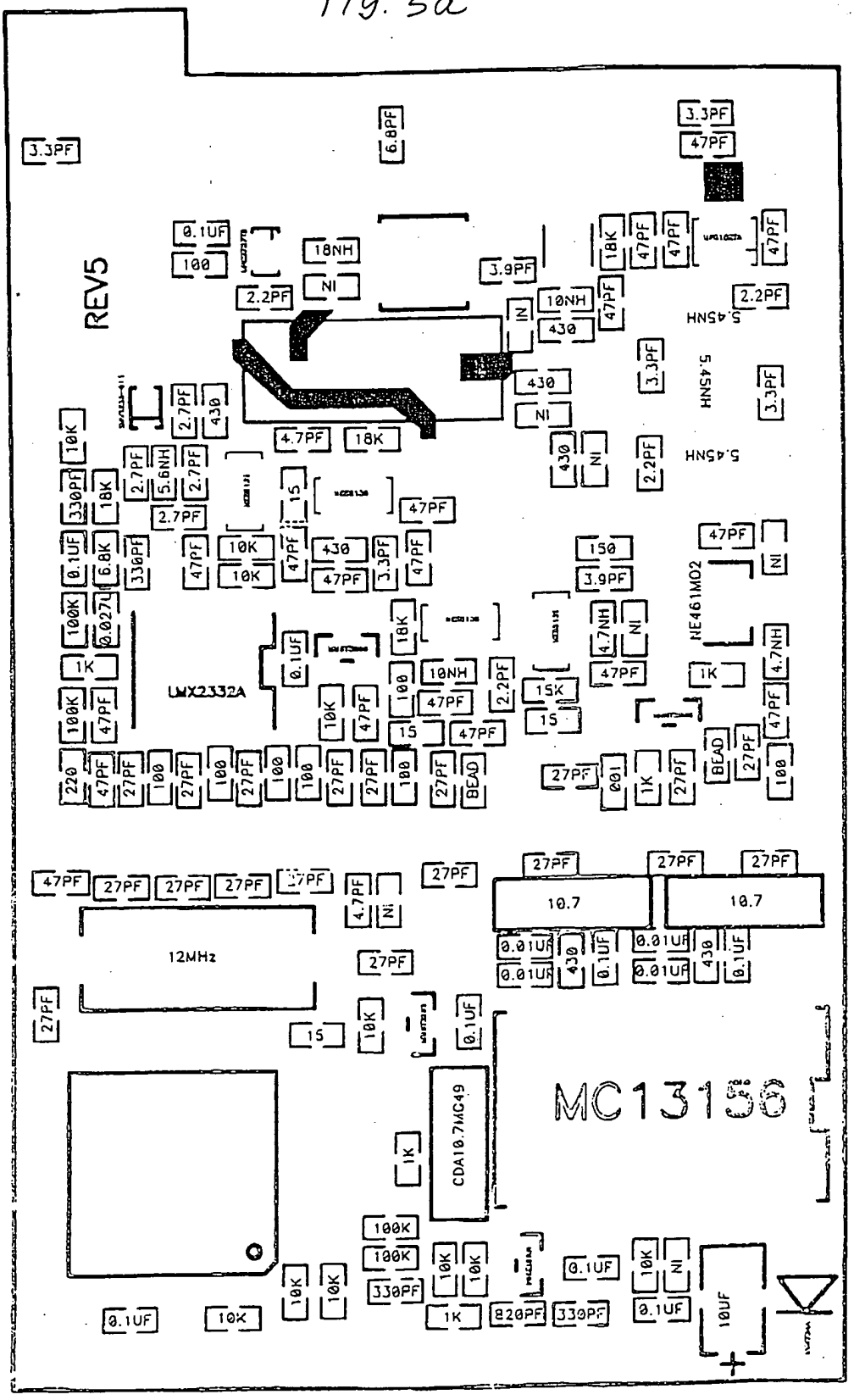
REV5
LMX2332A
NE461M02
MC13136
12MHz
CDA10.7MG49
10.7
10.7
3.3PF
6.8PF
47PF
0.1UF
100
18NH
NI
2.2PF
3.9PF
18K
10NH
430
5.45NH
4.7PF
2.7PF
5.6NH
330PF
0.1UF
6.8K
0.027U
100K
1K
10K
15
150
4.7NH
27PF
220
BEAD
0.01UF
10UF
820PF

Fig. 5b

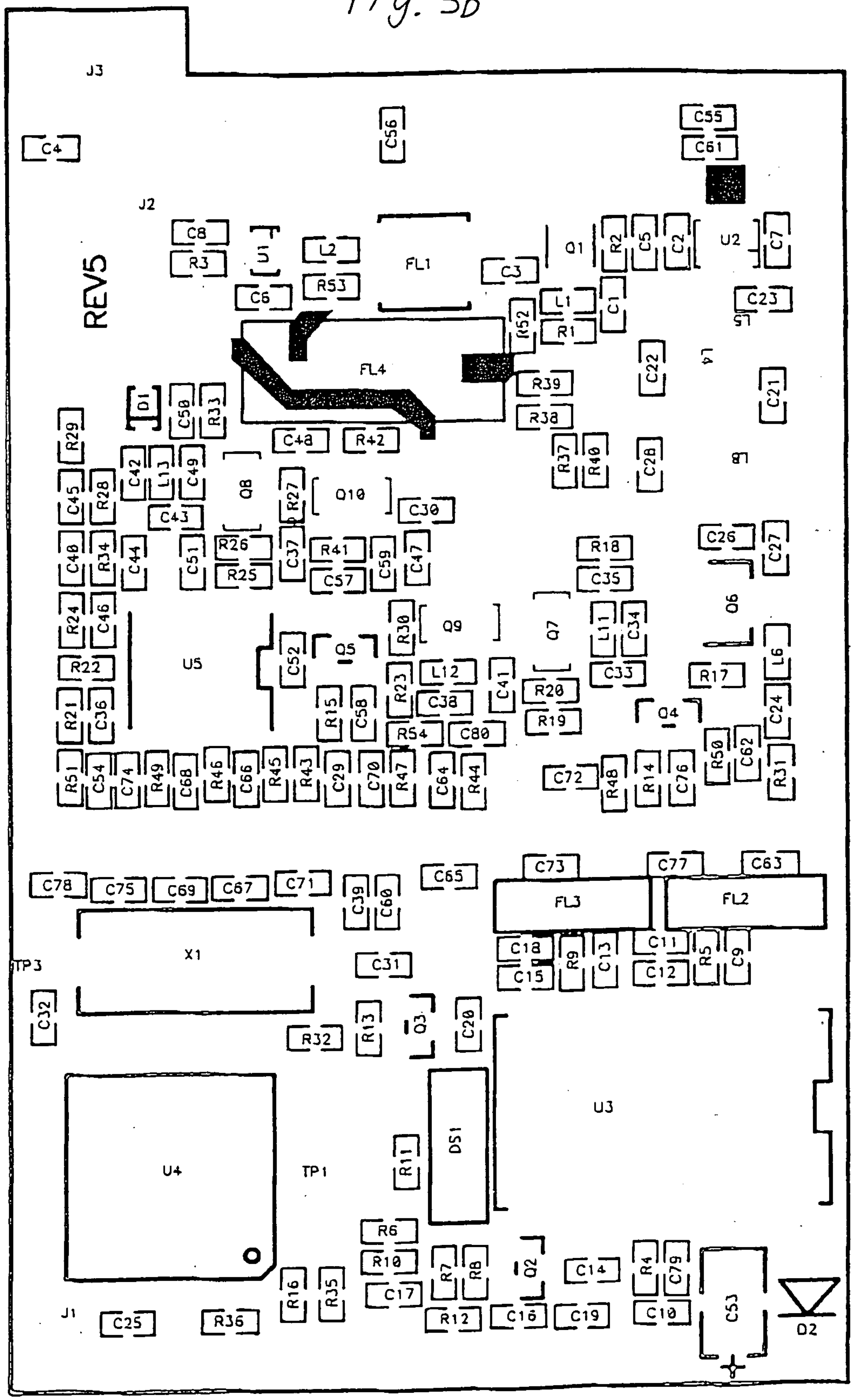
J3
C4
C56
C55
C61
J2
REV5
C8
R3
U1
L2
R53
FL1
C3
Q1
R2
C5
C2
U2
C7
C6
C23
L1
C1
R52
R1
L5
FL4
L4
C22
R39
R38
C21
D1
C50
R33
C48
R42
R37
R40
C28
L8
R29
C42
L11
C49
Q8
R27
Q10
C30
C45
R28
C43
R26
C37
R41
C59
C47
R18
C26
C27
C40
R34
C44
C51
R25
C57
C35
R24
C46
R30
Q9
Q7
L11
C34
Q6
U5
C52
Q5
L6
R22
R23
L12
C41
R20
C33
R17
C38
Q4
C24
R21
C36
R15
C58
R19
R54
C80
R50
C62
R51
C54
C74
R49
C68
R46
C66
R45
R43
C29
C70
R47
C64
R44
C72
R48
R14
C76
R31
C73
C77
C63
C78
C75
C69
C67
C71
C39
C60
C65
FL3
FL2
X1
C18
R9
C13
C11
R5
C9
TP3
C15
C12
C31
C32
R32
R13
Q3
C20
U3
DS1
U4
TP1
R11
R6
R10
R7
R8
Q2
C14
R4
C79
R16
R35
C17
C53
D2
J1
C25
R36
R12
C16
C19
C10

Fig. 5c

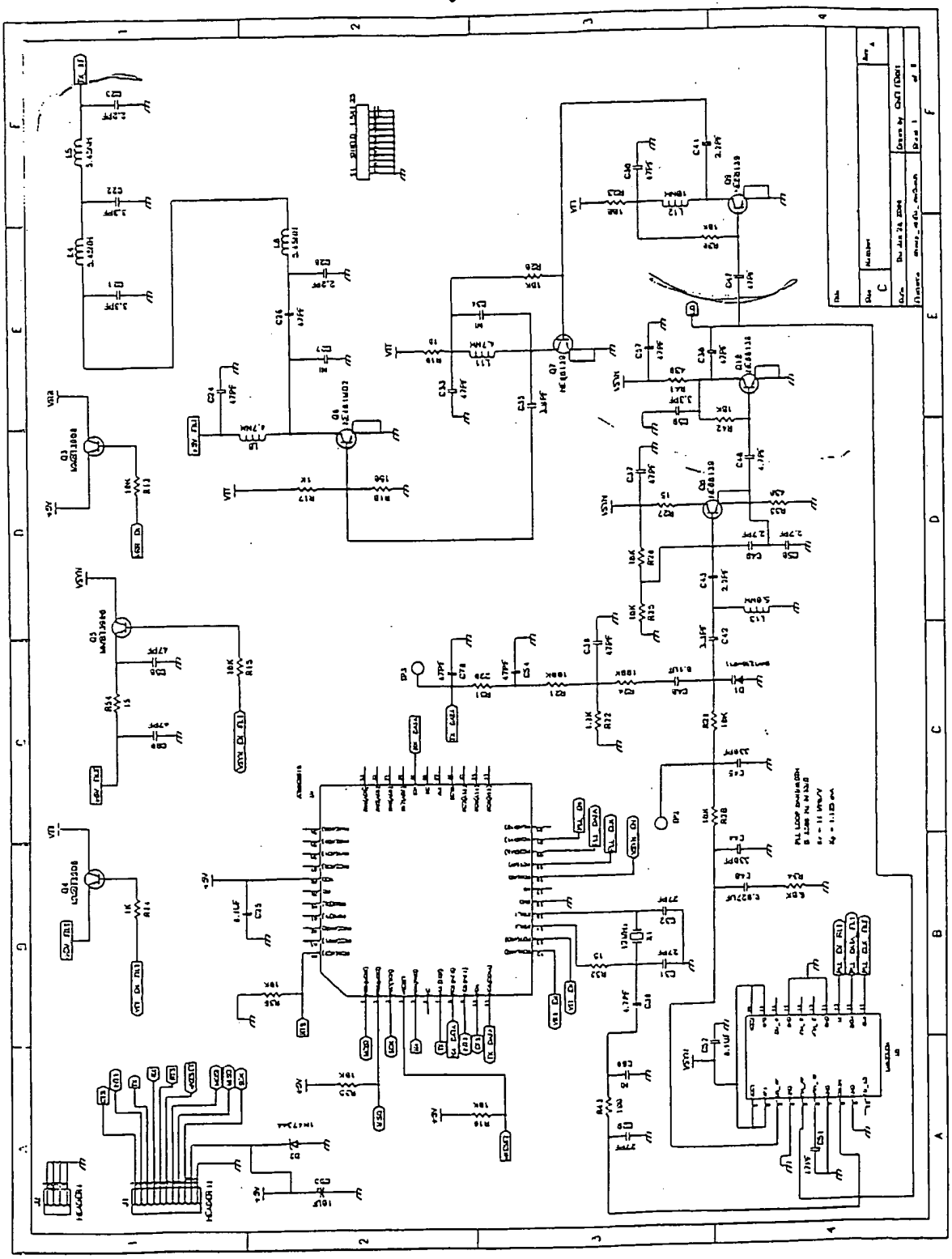

Fig. 5d